Employing Risk Management Techniques to Mitigate Technological and Market Pitfalls

The Challenges and Realities of High-Performance and Low Power SoC Designs

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Abstract

This paper examines the challenges of high-performance and low power System-on-Chip (SoC) designs and examines some risk management techniques used to help manage the complex technology and market demands. It also discusses the role a trusted semiconductor IP partner plays in helping customers navigate the risks and development costs by adopting standards-based, production proven technology.

INTRODUCTION

Market Challenges Overview – The Driving Factors

In today's hyper competitive markets the challenge of being first to market with the right product is an important element in the success of your business. Equally as important is being able to deliver a high quality product to the market, and ensuring that the features selected and implemented are the correct ones, and that the cost of getting to market with the right product and features is minimal.

Since tastes and technology change rapidly, these are difficult challenges to achieve. To help management and engineers meet these challenges, they must employ risk management techniques to mitigate technological and market pitfalls.

The R&D cost of SoCs in advanced process nodes grows exponentially and dictates stricter design and verification methodologies to help mitigate risk. Verification costs have surpassed development costs – and the gap continues to broaden with skyrocketing technology development and wafer costs.

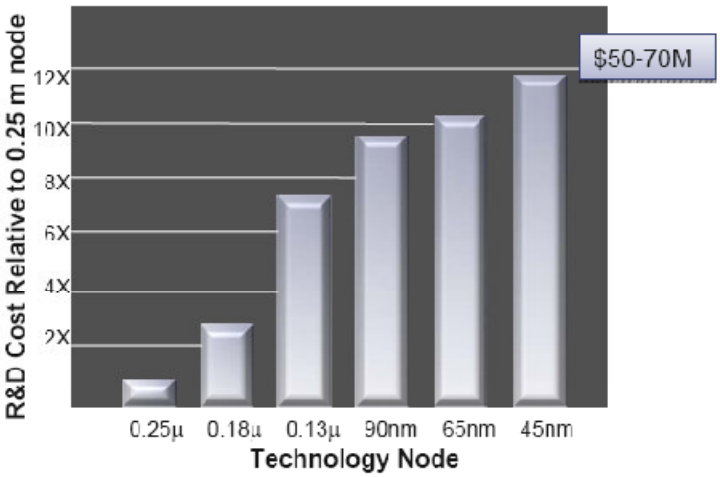

Figure 1. Total R&D Cost Versus Technology Node Relative to Cost at 0.25µm
(Source: Dr. Morris Chang, TSMC)

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Consumer Requirements vs. Technological Challenges
In the electronics market, the end user evaluates and selects products based on their attractiveness, functionality and cost. In a typical consumer device, high-performance features and battery life are keys to the consumer's decision to purchase the device.

In many applications the data, video and audio streams have doubled in rate and the need for storage capacity has increased rapidly to satisfy the technological advancements and the demand for live multimedia access at any time and any place.

The convergence in home electronics also adds complexity to the design of devices and systems as the transition from traditional consumer electronics with a single prime use turn into devices that are always connected and support multiple application platforms. For example, laptops, netbooks and smart phones can serve similar functionality, and when used at home can benefit from connectivity to traditional home appliances such as a High-Definition TV set for a complete experience.

The traditional implementation of processor core and parallel bus cannot satisfy the demand for high-performance while maintaining a reasonable power budget. Driving processors to achieve increasingly higher performance with rich feature sets results in exponentially higher power consumption. The power and performance specifications of parallel buses have challenged achieving economical and power friendly implementation for many advance interfaces.

These trends transformed the processor core implementation from single to multi core, and on the interface from parallelism to serialization.

The implementation of serial interface enables achieving very high-performance standard interfaces such as PCI Express, SATA, MIPI, HDMI and DisplayPort. Serial interface design is complex but can achieve performance and meet targets successfully.

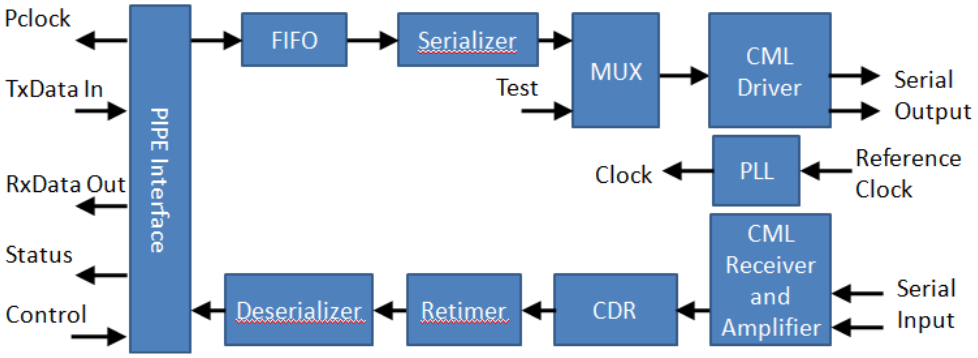

Figure 2. PCI Express PHY Block Diagram Example

Meeting the power budget is achievable with a SerDes (serializer – deserializer) implementation, as compared to a parallel interface with multiple wires switching simultaneously, that consumes more power, complicates board design, and adds signal integrity complexity.

The Need for Interface IP
As processor designs require more high-performance and low power interfaces, the demand for off-the-shelf standards-based interfaces is increasing. When standards such as PCI Express, HDMI, DisplayPort or MIPI are involved, the differentiation between vendors is minimized and the focus is on features that can differentiate from the competition.

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Furthermore, since the design of high speed standards-based SerDes PHY is complex, the benefit from designing it internally diminishes. The estimated development of standard-based PCI Express Gen2 PHY is about 40 man years, which is a substantial amount of time with no certainty of first time success. As process nodes continue to evolve, meeting the cost, power, performance requirements, makes the design even more challenging.

These reasons can bias the "make versus buy" decision towards acquiring the standards-based interface solution from an IP vendor rather than allocating internal resources to develop a building block that provides little or no added value when competing in the market.

Developing MIPI or PCI Express PHYs internally can potentially expose the company to unnecessary risks when a reasonable alternative exists in acquiring third-party proven technology that meets all standards and requirements. It becomes a clearer decision to make.

Uncertainty Surfaces with Multimedia Interfaces

There is an uncertainty in the market regarding multimedia interfaces. HDMI is the de-facto standard for consumer electronics with its adoption in TVs, multimedia electronics, and even in smart phones. Alternatively, DisplayPort is an open industry standard promoted by the Video Electronics Standards Association (VESA) that is supported by many companies. The DisplayPort standard was introduced by leading electronic manufacturers mainly in the computing and display applications and can be considered as aiming at dispelling the dominance of HDMI in the future.

The fact that laptops and desktops today offer DisplayPort transmitter interfaces helps create consumer demand for consumer appliances with receiver capability in order to connect the computing device to consumer appliances at home to broadcast multimedia. The belief is that this convergence will require the adoption of DisplayPort in addition to HDMI in the short term for the consumer electronics market. But can these standards live together?

Typically SoC architectural decisions are made early in the design cycle, and the decision regarding what standards to implement is made several months before tape out. A typical cycle can take more than a year, and approximately two years until the SoC actually reaches the harsh reality of the market.

As markets evolve, and particularly with respect to DisplayPort and HDMI, the uncertainty and risk of designing with HDMI but not DisplayPort – or vice-versa – can impact the success of the product and even the future of a company.

Meeting the Market Needs with a New Class of IP

Balancing the demands for faster, lower power and lower cost devices and systems, along with resource allocations for differentiating tasks vs. standard tasks to outsource or acquire, is part of the formula to achieve success. Partnering with a trusted IP provider enables rapid market penetration and the assurance that first silicon works to specifications.

The engineering risks and the time it takes to design and verify a design, while still meeting power, performance and budget constraints for a SoC are coupled with market direction uncertainty, and it requires careful planning of internal and external resources. Electing to outsource (or in another words IP licensing), standards-based IP components makes the most sense from an economical and risk mitigation perspective. However, choosing the IP vendor that provides a sure path to first silicon success is not easy to find, especially at advanced process nodes.

As the semiconductor industry's trusted IP partner, and leading provider of production proven interface IP solutions, Virage Logic has introduced a new class of IP that is used in AMD graphics and application processors. With production volume exceeding 100 Million units in total silicon shipments over multiple process nodes and products, Virage Logic's SiPro™ interface IP product line offers confidence with regard to first silicon success and yield optimization

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Figure 3. 40nm AMD/ATI Radeon Graphics Processor

Virage Logic's SiPro product line delivers a broad product portfolio of production-proven PHYs and controllers for PCI Express, MIPI, HDMI, DVI and DisplayPort, targeting high volume applications.

The Universal multimedia IP solution supporting dual-mode HDMI and DisplayPort interfaces enables a "future-proof design" by offering both DisplayPort and HDMI capabilities to help alleviate concerns over the decision to select one option over the other. The Universal HDMI/DVI/DisplayPort IP approach allows the same design to be easily targeted to either of these standards, enabling customers to make decisions late in the design cycle for maximum flexibility.

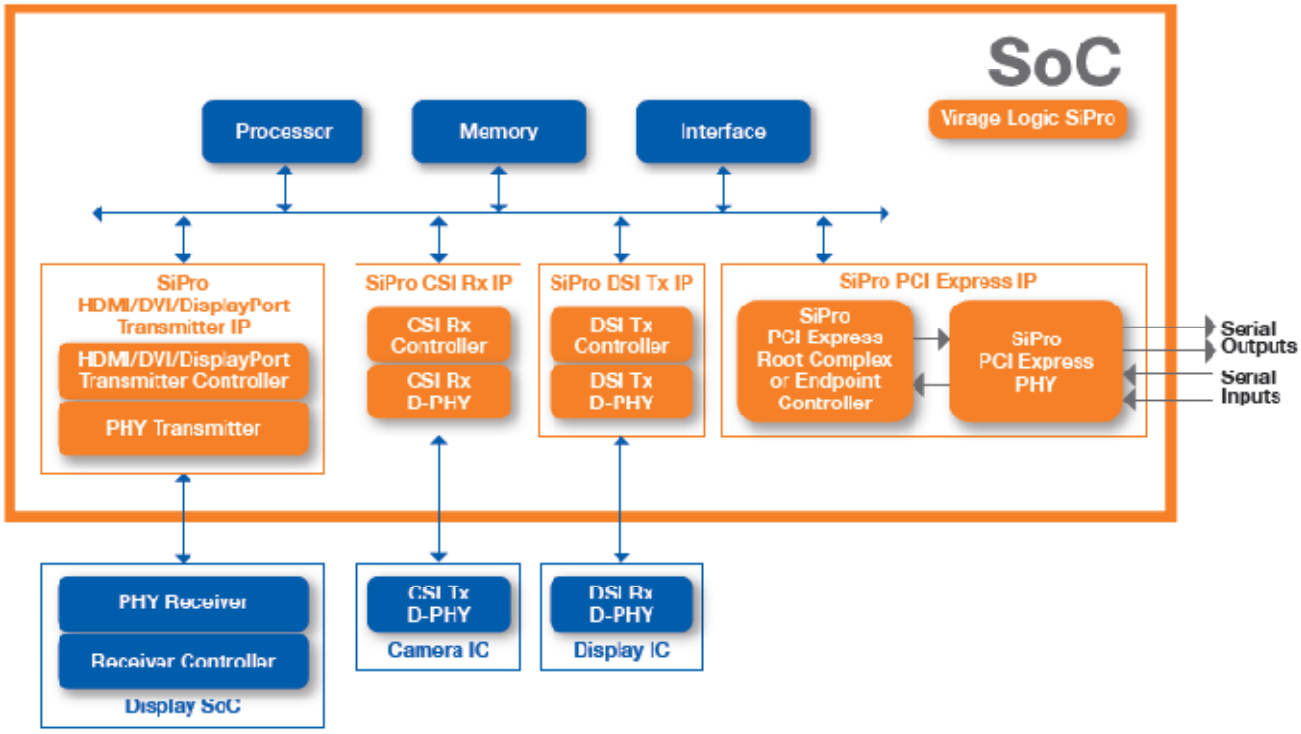

Figure 4. Virage Logic's SiPro Advanced Interface IP Solutions

About Virage Logic's SiPro Product Line

Virage Logic's SiPro product line of advanced interface IP helps to manage complex design technology and market demands. The SiPro products are optimized for mass production, and are rigorously verified and characterized to help reduce risk, improve time-to-market, and maximize yield; meeting the difficult challenges of high-performance and low power SoC designs with standards-based, production-proven advanced interface IP solutions.

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If you have further questions regarding the SiPro product line, please contact Virage Logic.

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